LAYOUT OF A FLASH MEMORY HAVING SYMMETRIC SELECT TRANSISTORS

ABSTRACT OF THE DISCLOSURE

A layout of flash memory having symmetric select transistors includes a memory cell array and a polysilicon gate. The polysilicon gate forms a plurality of select transistors in coordination with a plurality of pairs of sources/drains, so as to connect to the memory cell array. The polysilicon is perpendicularly extended toward a direction of the memory cell array, thereby overcoming a drawback as select transistors being unsymmetrical in a prior flash memory structure.